REMARKS/ARGUMENTS

Claims 1-22 are pending. Claims 1-22 are rejected. Applicants respectfully request further examination and reconsideration in view of the instant response. No new matter has been added herein as the result of the amendments.

Amendments to Claims

Claim 1 has been amended to reflect the following (Claims 8 and 14 include similarly amended features):

> A circuit for a memory module address bus comprising:
>
> a transmission line comprising a dampening impedance between a driver and a branch point of said transmission line; and
>
> a parallel termination impedance having one end coupled to said transmission line between said series dampening impedance and said branch point, wherein said parallel termination impedance is on the same side of any memory module as said driver;
>
> said transmission line having branches from said branch point, wherein ones of said branches are coupled to at least one memory module interface.

Support for the amendment, "wherein said parallel termination impedance is on the same side of any memory module as said driver" can be found in Applicants' specification at least on page 9, lines 16-24.

Claims 1, 6-8, 14, and 20-22 have been amended to reflect consistent usage of the following terms: parallel termination impedance, and series dampening impedance. These terms are used in Applicants' specification at least on page 9, lines 1-15.

CLAIM REJECTIONS

Double Patenting

The Office Action mailed June 11, 2008 (hereinafter, "instant Office Action") states that Claims 1, 2, 7-10, and 12-16 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over Claims 1, 2, 7-10, and 12-16 of U.S. Patent Application No. 7,207,862.

A terminal disclaimer in compliance with 37 CFR §1.321(c) is being submitted concurrent with the instant response, thereby obviating the double patenting rejection.

Claim Objections

The instant Office Action states, "Claim 14 is objected to because of the following informalities: There is insufficient antecedent basis for the limitation 'dampening impedance' on line 6 of claim 14… Appropriate correction is required" (instant Office Action, page 4, fourth paragraph). Applicants have amended Claim 14 to refer to "series dampening impedance" instead of "series impedance". Therefore, Applicants respectfully submit that Claim 14 traverses the instant Office's objection and is thus in condition for allowance.

Similarly, the instant Office Action objected to Claim 22 as having insufficient antecedent basis for the limitation "series resistance" and required appropriate correction. Applicants respectfully submit that Claim 22 has been amended appropriately and therefore traverses the instant Office's objection, thus being in condition for allowance.

Rejection under 35 U.S.C. §102(e)

Claims 1-5, 7-19 and 21

The instant Office Action states that Claims 1-5, 7-19, and 21 are rejected under 35 U.S.C. §102(e) as being anticipated by Johnson et al. (U.S. Patent Application No. 6,715,014) (hereinafter, "Johnson"). The rejections and comments set forth in the instant Office Action have been carefully considered by the Applicants. Applicants respectfully submit that Claims 1-5, 7-19, and 21 are not anticipated by Johnson in view of at least the following rationale.

Applicants respectfully point out that amended Claim 1 recites (Claims 8 and 14 include similar features):

> A circuit for a memory module address bus comprising:
>
> a transmission line comprising a dampening impedance between a driver and a branch point of said transmission line; and
>
> a parallel termination impedance having one end coupled to said transmission line between said series dampening impedance and said branch point, wherein said parallel termination impedance is on the same side of any memory module as said driver;
>
> said transmission line having branches from said branch point, wherein ones of said branches are coupled to at least one memory module interface.

Applicants respectfully note, "[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference". MPEP §2131; *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 103 (Fed. Cir. 1987). … "The identical invention must be shown in as complete detail as is contained in the … claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9

USPQ2d 1913, 1920 (Fed. Cir. 1989). "The elements must be arranged as required by the claim..." *In re Bond*, 910 F.2d 831, 15 USPQ2d 1913, 1920 (Fed. Cir. 1989).

The instant Office Action states that:

> Figure 3 of Johnson discloses a circuit for a memory module address bus comprising:...a transmission line (314) comprising a dampening impedance (324) between a driver (312) and a branch point (node between 318 and 320, hereinafter "star node") of said transmission line (314); and
> a termination impedance (326) having one end coupled to said transmission line (314) between said dampening impedance (324) and said branch point (star node);
> said transmission line (314) having branches (316-322) from said branch point, wherein ones of said branches are coupled to at least one memory module interface (304).

(Emphasis added; instant Office Action, page 5, last paragraph, through page 6, first and second paragraphs.)

Applicants respectfully submit that Johnson does not anticipate "a parallel termination impedance having one end coupled to said transmission line between said series dampening impedance and said branch point, wherein said parallel termination impedance is on the same side of any memory module as said driver" (Emphasis added; Applicants' Claim 1.) Applicants understand Johnson, and more specifically Johnson's Figure 3, to disclose termination impedance that is not between the branch point and the dampening impedance.

Therefore, Applicants respectfully submit that Johnson does not anticipate "a parallel termination impedance having one end coupled to said transmission line between said series dampening impedance and said branch point, wherein said parallel termination impedance is on

the same side of any memory module as said driver" (emphasis added) as is recited in Applicants' Claim 1.

Therefore, Applicants respectfully submit that Johnson does not anticipate the features as are set forth in independent Claim 1, and as such, Claim 1 traverses the rejection under 35 U.S.C. §102(e) and is condition for allowance. Accordingly, Applicants also respectfully submit that Johnson does not anticipate Claims 8 and 14 for reasons stated herein regarding Claim 1. Furthermore, Applicants respectfully submit that Claims 2-5 and 7 depending on Claim 1, Claims 9-13 depending on Claim 8, and Claims 15-19 and 21 depending on Claim 14 overcome the rejection under 35 U.S.C. §102(e) as being dependent on an allowable base Claim.

Rejection under 35 U.S.C. §103(a)

Claims 6 and 20

The instant Office Action rejected Claims 6 and 20 under 35 U.S.C. §103(a) as being unpatentable over Johnson in view of Buuck et al. (U.S. Patent Application No. 5,583,449) (hereinafter, "Buuck"). The rejections and comments set forth in the instant Office Action have been carefully considered by the Applicants. Applicants respectfully submit that Claims 6 and 20 are patentable over Johnson in view of Buuck for at least the following rationale.

Applicants respectfully submit that the combination of Johnson and Buuck does not satisfy the requirements of a *prima facie* case of obviousness because the features of Claims 6 and 20 as a whole would not have been obvious over the combination of Johnson and Buuck.

"As reiterated by the Supreme Court in *KSR*, the framework for the objective analysis for determining obviousness under 35 U.S.C. 103 is stated in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966). Obviousness is a question of law based on underlying factual inquiries" including "[a]scertaining the differences between the claimed invention and the prior art" (MPEP 2141(II)). "In determining the differences between the prior art and the claims, the question under 35 U.S.C. 103 is not whether the differences themselves would have been obvious, but whether the claimed invention as a whole would have been obvious" (emphasis in original; MPEP 2141.02(I)).

Applicants respectfully note that "[t]he prior art reference (or references when combined) need not teach or suggest all the claim limitations. However, Office personnel must explain why the difference(s) between the prior art and the claimed invention would have been obvious to one of ordinary skill in the art" (emphasis added; MPEP 2141[III]).

As presented above, Applicants respectfully submit that Johnson does not teach "a parallel termination impedance having one end coupled to said transmission line between said series dampening impedance and said branch point, wherein said parallel termination impedance is on the same side of any memory module as said driver" (emphasis added) as is recited in Applicants' Claim 1. Applicants' specification describes at least one advantage for the positioning of its parallel termination impedence: "[a]s positioned, the combination of the series dampening impedance 350 and the parallel termination impedance 360 prevents, or at least reduces, reflections from the memory modules 340 from travelling back to the driver 305 in the

region of the transmission line 320a between the parallel termination resistor 360 and the driver 305" (Applicants' specification, page 9, lines 21-23, through page 10, lines 1-3).

In contrast, Johnson's termination impedance is not in between the dampening impedance (324) and the branch point, and is on the same side as any memory module (302, 304, 306, and 308) as a driver (312). (See Johnson's Figure 3.) Furthermore, Applicants respectfully submit that the combination of Johnson and Buuck fails to suggest the features of Applicants' Claim 1 as a whole.

Applicants understand Buuck to teach the "cancellation of line reflections in a clock distribution network" (Buuck, Title.) Specifically, Buuck does not teach, describe, or suggest "a parallel termination impedance having one end coupled to said transmission line between said series dampening impedance and said branch point, wherein said parallel termination impedance is on the same side of any memory module as said driver" (emphasis added) as is recited in Applicants' Claim 1.

Additionally, Applicants respectfully submit that the instant Office Action does not explain why the differences between Johnson, Buuck, and Applicants' claimed features would have been obvious to one or ordinary skill in the art.

Thus, in view of the combination of Johnson and Buuck not satisfying the requirements of a *prima facie* case of obviousness, Applicants respectfully assert that Claim 1 is patentable. Furthermore, Applicants respectfully submit that Claim 14 is also patentable for reasons stated

herein regarding Claim 1. Moreover, Applicants respectfully submit that Claim 6 depending on Claim 1, and Claim 20 depending on Claim 14 are patentable as being dependant upon an allowable base Claim.

Claim 22

The instant Office Action rejected Claim 22 under 35 U.S.C. §103(a) as being unpatentable over Johnson in view of Mizukami et al. (U.S. Patent Application No. 5,111,080) (hereinafter, "Mizukami"). The rejections and comments set forth in the instant Office Action have been carefully considered by the Applicants. Applicants respectfully submit that Claim 22 is patentable over Johnson in view of Mizukami for at least the following rationale.

Applicants respectfully submit that the combination of Johnson and Mizukami does not satisfy the requirements of a *prima facie* case of obviousness because the features of Claim 22 as a whole would not have been obvious over the combination of Johnson and Mizukami.

As presented above, Applicants respectfully submit that Johnson does not teach or suggest "a parallel termination impedance having one end coupled to said transmission line between said series dampening impedance and said branch point, wherein said parallel termination impedance is on the same side of any memory module as said driver" (emphasis added) as is recited in Applicants' Claim 1. Furthermore, Applicants respectfully submit that the combination of Johnson and Mizukami fails to suggest the features of Applicants' Claim 1 as a whole.

Applicants understand Mizukami to teach the a "complementary signal transmission circuit with impedance matching circuitry" (Mizukami, Title.) Specifically, Mizukami does not teach, describe, or suggest "a parallel termination impedance having one end coupled to said transmission line between said series dampening impedance and said branch point, wherein said parallel termination impedance is on the same side of any memory module as said driver" (emphasis added) as is recited in Applicants' Claim 1.

Additionally, Applicants respectfully submit that the instant Office Action does not explain why the differences between Johnson, Mizukami, and Applicants' claimed features would have been obvious to one or ordinary skill in the art.

Thus, in view of the combination of Johnson and Mizukami not satisfying the requirements of a *prima facie* case of obviousness, Applicants respectfully assert that Claim 1 is patentable. Furthermore, Applicants respectfully submit that Claim 14 is also patentable for reasons stated herein regarding Claim 1. Moreover, Applicants respectfully submit that Claim 22 depending on Claim 14 is patentable as being dependant upon an allowable base Claim.

CONCLUSION

In light of the above-listed remarks, the Applicants respectfully request allowance of the claims 1-22.

The Examiner is urged to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

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Date: 09/10/2008

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